In the Specification

The paragraph beginning at line 10 on page 2 has been amended as follows:

The FETs used as access transistors determine some of these other concerns. The FETs need to be able to provide a high impedance when they are turned OFF, and a low impedance connection when they are turned ON. DRAMs and other memories use an addressing scheme whereby a wordline that is coupled to many transistor gates is selected, and at the same time a bitline or digitline that is coupled to many transistor drains is also selected. A FET that is located at the intersection of the selected wordline and the selected bitline is turned ON, and that memory cell is accessed. At the same time, many other FETs have a drain voltage due to the drains of these FETs being coupled to the selected bitline. These FETs exhibit some parasitic conductance as a result of the drain voltage. In some types of integrated circuits, a portion of that parasitic conductance is due to corner effects that are an artifact of using ~~Trench~~ trench isolation techniques to isolate the FETs from one another and from other circuit elements.

The paragraph beginning at line 14 on page 7 has been amended as follows:

In one embodiment, the first angle θ_1 is less than about sixty degrees and the second angle θ_2 is eighty degrees or more. In one embodiment, the first angle θ_1 is in a range of from about five degrees to about forty-five degrees. In one embodiment, the first angle θ_1 is ~~in~~ about thirty-five degrees. In one embodiment, the first angle θ_1 is about forty degrees. The concerns addressed in selecting the first angle θ_1 are to select an angle θ_1 providing a shoulder that reduces electrical fields in the subsequently-formed FET 12 and to also select an angle that does not impede subsequent filling of the trench isolation structures 10 with dielectric material such as silicon dioxide.